Application No.: 10/665,289 Docket No.: 21806-00056-US1

AMENDMENTS TO THE CLAIMS

This listing of claims replaces all previous versions and listings of claims in this application.

Claim Listing:

Claims 1-28 (Cancelled).

29. (Currently amended) A method for offloading hardware interrupt processing from a host system to a subsystem comprising:

capturing, in a subsystem memory ~~as an executable program~~, hardware instructions generated by high-level specifications of operations in a computer program;

generating an executable program from the captured hardware instructions and storing the executable program in the subsystem memory;

utilizing a subsystem processor to ~~issue said captured instructions from said memory to~~ execute the executable program with subsystem hardware without hardware interrupt processing by the host system;

wherein said subsystem hardware includes a status indicator containing status information relating to a plurality of operations being carried out on said subsystem hardware,

wherein said subsystem processor monitors said status indicator and issues said captured instructions in response to said status information.

30. (Previously presented) The method of claim 29 wherein said captured programs include an instruction for causing said subsystem processor to delay issuing instructions in said captured programs until said status indicator contains specified status information.

31. (Previously presented) The method of claim 30 wherein said specified status information relates to the completion of a specified operation.

32. (Previously presented) The method of claim 31 wherein said operation is repeated periodically.

33. (Previously presented) The method of claim 31 wherein said operation is one of a plurality of operations which are performed serially.

34. (Currently amended) A computer system suitable for graphics rendering, comprising:

a host system including at least a CPU and a system memory, said host system providing hardware instructions generated by high-level graphics operations executed by the host system;

a graphics subsystem operatively coupled to the host system,

wherein said graphics subsystem contains a display list processor operatively connected to a graphics accelerator,

wherein said graphics accelerator includes a plurality of status registers which each indicate a status of a different one of a plurality of graphics operations,

wherein said graphics subsystem receives the hardware instructions provided by the host system,

wherein said graphics subsystem uses the hardware instructions to generate an executable program that is stored in a subsystem memory, and

wherein ~~and reduces a requirement for~~ hardware interrupt generation and handling is accomplished by the graphics subsystem and not by the CPU.

35. (Previously presented) The computer system of claim 34, wherein at least one of the plurality of graphics operations are operations carried out by the graphics accelerator.

36. (Previously presented) The computer system of claim 34, wherein at least one of the plurality of graphics operations are operations carried out by a hardware device external to the graphics accelerator.

37. (Previously presented) The computer system of claim 34, wherein the plurality of graphics operations are serial operations.